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FIS9-2000-0362

09/827,026

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Reply to office action mailed 04/29/2004

REMARKS

Claims 1 - 15 are currently pending in the application. No claims have been amended, and the applicant requests reconsideration based on the remarks below. The undersigned thanks the Examiner for the indication that claims 9 and 10 are allowable, and believes that the Examiner will agree that claims 1-8 and 11-15 are also drawn to allowable subject matter based on the remarks.

Claims 1 - 4, 8 and 11 - 13 have been rejected under 35 U.S.C 102(e) as being anticipated by Williams (US Patent 6,714,021). This rejection is traversed.

With respect to claims 1 and 11 - 12, the Examiner states that Williams (6,714,021) is performing the same course and fine timing adjustments as the subject invention. This is incorrect. Williams deals with the Time Domain Reflection (TDR) techniques for locating transmission line faults. The subject invention is using course and fine timing adjustments to test an integrated circuit (e.g., access time, setup and hold time, cycle time, etc.). For example, access time is the time a device takes to locate a single piece of information and make it available to the computer for processing. The reference cited by the Examiner (Fig 15 and column 8, lines 12 - 29) discusses the sampling of voltage levels on a transmission line at course and fine timing instances to determine if there is voltage and not what the data on the line is. These sampling instances (also called TDR CLOCK) are created by the coarse time base (1220) and fine time base (1299) generators. That is, TDR CLOCK controls the instances when a 'picture' of the voltage is taken. This picture is compared to a reference voltage level to determine if a break in the transmission line has occurred.

This is significantly different from the subject invention which actually generates coarse and fine timing signals which are applied to the input/outputs (I/O) of the IC under test. The integrated circuit chip I/O is accessed at the intervals set by the timers to determine when the data is present. The interval is varied, first in a coarse timing interval and then in a fine timing interval. As recited in claim 1,

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“...a first timer for performing a coarse timing measurement.... a second timer for performing a fine timing measurement...”

These timing measurements are then stored for further analysis. By performing different analyses of the timing measurement, the access time, cycle time, etc. of the IC can be determined.

In addition, Williams varies the TDRLOCK signal relative to the time period for the reflected signal on the transmission line to subside (column 8, lines 2 - 5). The subject invention is using both coarse and fine timing intervals to determine precise measurements of the characteristics of the IC. This can not be provided by Williams as the timing intervals are not precise (column 7, lines 64 - 65 which states, “..TDRLOCK does not need precise control...”

In view of the above, claims 1, 11 and 12 are not anticipated by Williams, and the dependent claims thereon are also not anticipated.

Claims 5 - 7 and 14 - 15 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Williams (US Patent 6,714,021). This rejection is traversed.

The Examiner is equating delay elements of Williams with the control word of the subject invention. This is incorrect. Williams uses a series of D-type flip flops to delay the active state of when the voltage level on the transmission line is looked at. As recited in column 8, lines 18 - 23,

“... D-type flip-flops 1201 to 1215, coupled to a coarse time base multiplexer 1220 which selects the number of delay gates. Delay gates 1201 through 1215 may be any suitable delay elements but each should provide approximately equal delays. The total number of delay gates depends on the total delay required...”

This is different from the subject invention in that the subject invention uses control words to adjust or vary the fine and coarse timing intervals. It does not just delay when a timing instant occurs. As recited in the specification of the subject invention on page 7, beginning at line 26,

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“...CLK to **generate the control words** CNTL1 and CNTL2. As CLK is pulsed, the 4-bit outputs CNTRL1 and CNTRL2 are progressed through their counts.”

There is no progression of a control word or control word count in Williams.

Williams either delays or does not delay by a set value which is selected by the number of flip-flops in the circuit. Therefore, Williams can not control the adjustments to the fine and coarse timings using control words as does the subject invention.

Claims 1 and 11 - 12 have been rejected under 35 U.S.C. 102(e) as being anticipated by Dilger et al. (US Patent 6,161,420). This rejection is traversed.

Dilger is making a frequency measurement of an oscillator. The intent is to make a device to detect the presence of a gas by use of a piezoelectric acoustic wave device and detecting a change in its resonant frequency in the presence of a gas. Dilger has described a method where a continuously running oscillator is controlled by a quartz crystal microbalance (QCM) technique and produces a first oscillating signal. This first oscillation is coarsely measured and reproduced by a frequency synthesizer to generate a second oscillation. A difference signal is generated by comparing (multiplying) the first and second oscillations to generate an error signal. The error signal being proportional to the difference in cycles per second between the first and second oscillations. Measurement of the frequency of the first oscillating signal is made by combining the error signal with the second signal. In its use as a gas detector, when the frequency changes a predetermined amount from an initial frequency indicative of the absence of gas, an alarm signal is generated.

In the subject invention, a measurement technique is described where a time delay is established by a coarse digitally controlled timer and a pass/fail test is conducted by an on-chip test system to see if the output of a chip matches expected data. If the test is passed, a second test cycle is issued with the time delay incremented by a small amount by a second, fine time-delay element. However if the test fails,

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adjustments are made to the coarse timer in subsequent tests until a pass condition is achieved. Fine adjustment to the timing interval under test is then made until the chip fails to output expect test data. The final setting of the digital delay elements are stored and are indicative of the timing margin of the chip timing parameter under test.

Furthermore, Dilger makes a course measurement of an input frequency then produces a reference frequency from a frequency synthesizer. The subject invention does not measure any frequencies, but does test for expect data at a known time delay.

Nor does the subject invention utilize a frequency synthesizer to generate a reference frequency. Dilger uses a subtraction circuit to measure the difference between an input frequency and the synthesized frequency. The subject invention does not work with frequency and does not have a subtraction element which outputs the difference between two frequencies. The circuit elements described in the Dilger claims can not be adapted to measure the timing margin of an integrated circuit. The Dilger apparatus requires a repeating oscillating signal to produce a measurement.

Specifically, the digital filter comprised of elements 126 and 130 in Figure 2 requires a continuously running oscillation input to produce the signal '164' of Figure 3.

Signal '164' is filtered by averaging several cycles to produce '166' and '168'. Signal '168' is a necessary and critical input to reconstruction circuit '138' in figure 2.

Without a repetitive (continuously) running input signal, the Dilger system will not operate. The subject invention test method for an integrated circuit makes a pass/fail decision of chip operability based on a single cycle.

In view of the foregoing, it is requested that the application be reconsidered, that claims 1- 15 be allowed, and that the application be passed to issue.

If for any reason Examiner remains of the position that Williams is applicable ~~to~~ to any of the claims, the undersigned has included a declaration herewith which ~~x~~ demonstrates prior invention by the applicant.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at 703-787-9400

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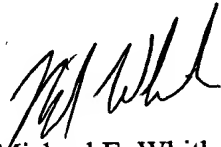
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(fax: 703-787-7557; email: mike@wcc-ip.com) to discuss any other changes deemed necessary in a telephonic or personal interview.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-2041 (Whitham, Curtis & Christofferson, P.C.).

Respectfully submitted,



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Please associate this
Application with
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FIS9-2000-0362

09/827,026

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



In re patent application of:

Wayne F. Ellis et al.

Confirmation No.: 4853

Serial No. 09/827,026

Group Art Unit: 2115

Filed: 04/05/2001

Examiner: Butler, Denise

For: AUTOMATIC TIMING ANALYZER

Box Non-Fee Amendment
Commissioner for Patents
Alexandria, VA 22313 - 1450

DECLARATION UNDER 37 C.F.R. 1.131
OF
JOHN FIFIELD

Sir:

John Fifield declares as follows:

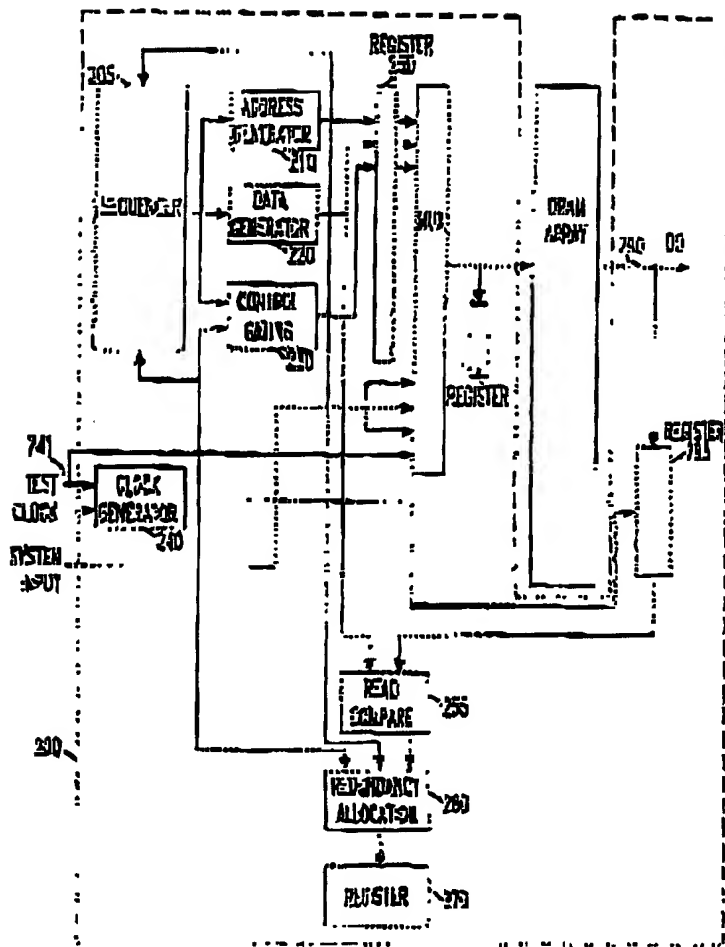
1. I am a joint inventor of the above-identified application, and I am currently employed by IBM Corporation, which I understand to be the Assignee of the above-identified application.
2. Attached as Exhibit 1 are copies excerpted pages from two IBM invention disclosures, both of which were prepared prior to January 11, 2001. I participated in the preparation of both disclosures prior to January 11, 2001, and reviewed the completed disclosures prior to January 11, 2001.
3. All acts related to the preparation of the pages in Exhibit 1, and any designing and testing discussed therein, were performed in the United States.
4. To the best of my knowledge, Exhibit 1 describes the invention claimed in the above-identified application. In particular, with respect to claim 1, the third page

of the disclosure states the following: "The first timer provides coarse timing adjust, while the second timer provides a fine timing adjust", and "At this point, the access time of the chip including the timing index of the coarse and fine timer are recorded in the tester". With respect to claim 2, the third page of the disclosure states "A built-in self-test (or so called BIST) algorithm is established for auto-analysis of the access time is shown in Figure 1" (see also Figure 1 on the fourth page). In addition, the fourth page indicates "Each clock period is a single test also issued by the BIST circuit". With respect to claim 5, the fourth page indicates "we use the two four bit counters to generate 16 intervals per timer. One can use 3 bit or 5 bit counter if the interval needs to be reduced or increased". With respect to claims 3-5, the fifth page states "C1, C2, C3, C4 are output digits from the coarse timer. For example, when C1=1, C2=1, C3=0, and C4=0, then at timing of 3X of the unit delay time is produced at output "SIG1". With respect to claim 6, the sentence bridging pages 3 and 4 states "one can start with a pass state then decrements the index till the chip fails." With respect to claim 7, Figure 2 on page 7 shows the four bit counters.

5. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the above-referenced application and any patent issuing thereon.

Date July 14 2004

John Fifield
John Fifield



4. If the invention is implemented in a product or prototype, include technical details, purpose, disclosure details to others and the date of that implementation.

**Main Idea for Disclosure BUR8-2000-0464**

Prepared for and/or by an IBM Attorney - IBM Confidential

Archived On 10/25/2000 01:02:11 AM

Title of disclosure (in English)

eDRAM#2: Automatic Timing Analyzer

Main Idea

*Doc Created 8/31/2000
Completed "workable" 9/12/2000*

1. Describe your invention, stating the problem solved (if appropriate), and indicating the advantages of using the invention.

PROBLEM

Usually a bench tester is used to test the access time of a memory chip manually. The procedure is first to pick a reasonable access time to test the memory array at a certain temperature. If the array functions properly, then the array will be tested again with an access time shorter than the originally set time. However, if the array fails, the time is extended. The method is repeated until when the array functions properly at the minimum access time, but fails if the time is shortened by some time interval. The resolution of the time interval usually determined by the capability of the bench tester. Although, the bench tester can be programmed to perform access time analysis, this method is time consuming and of limited accuracy.

INVENTION

Therefore the first object of the invention is to propose a test methodology to conduct a automatic chip timing analysis in a coarse and a fine resolution steps. The further object of the invention is to design a timing adjustment circuits comprising a coarse timing adjustment, and fine timing adjustment for chip timing analysis. Another object of the invention is to equip the timer circuit with a counter, so that an incremental or decremental timing analysis can be carried out with a specific timing

step. Finally, an algorithm is proposed to provide an effective, low-cost and accurate timing analysis.

claim 2 A built-in self-test (or so called BIST) algorithm is established for auto-analysis of the access time is shown in Fig1. This is accomplished by integrating at least two timer circuits onto the chip, to perform the algorithmic access time measurement.

claim 1 The first timer provides coarse timing adjust, while the second timer provides a fine timing adjust.

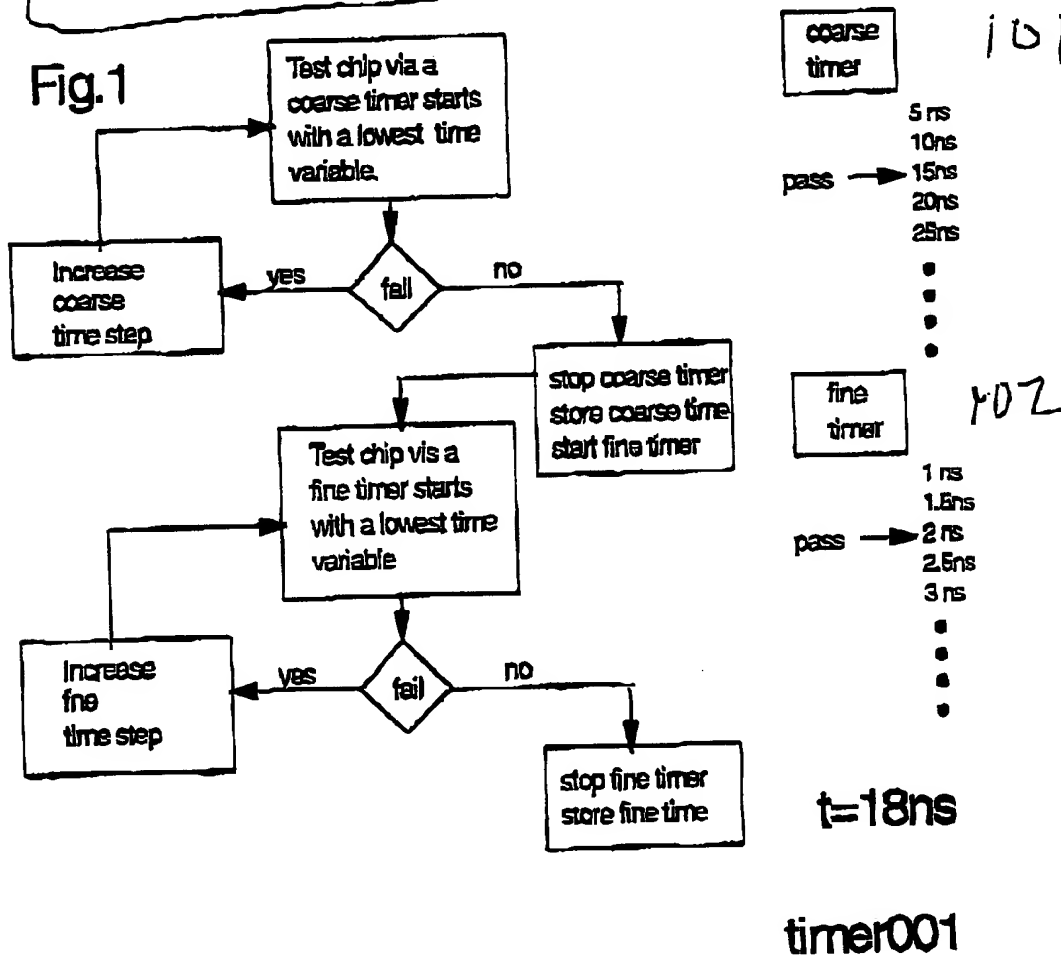
Extension of this concept to provide more timers with finer resolutions can be readily adapted without changing the concept of this proposal. For simplicity, only two timers are illustrated. We suggest to test the chip starting from a slower limit and decrease access time strobe setting by using the course timing adjust. For example, if the array is expected to have an access time at about 15ns to 20 ns, we pick 10ns to start the first run of testing. If the chip passes, the timer is incremented by one index of 5ns each time till it fails. If the chip fails at 15ns but passes at 20ns, at this moment the final fail state of the course timer is latched. In this case, 15ns timing index is stored in the tester. The chip is now tested using the fine timer starting at 15ns. The fine timer is set at an increment of 0.5 ns intervals each time of testing until the chip reaches its first pass.

claim 1 At this point, the access time of the chip including the timing index of the coarse and fine timer are recorded in the tester. As shown in Fig-1, in this example, an access time is the summation of 15ns (index recorded from coarse timer) +2ns (index recorded from the fine timer)=17ns, when the chip first passes the test. The timer settings are stored in a register and finally read out to show the final access time of the chip at a certain testing temperature.

claim 6 Based on the same concept many other similar algorithms can be carried out to conduct such automatic timing test. In stead of increment the timing index, one can start with a pass state then

claim 6
 decrements the index till the chip fails. Or, one can program the tester to perform test using the coarse timer with increment, while the fine timer with decrement, or vice versa. One can also starts testing from any arbitrary starting point, especially during fine time testing by either increment method or decrement method depending on the pass or fail result of the testing.

claim 5
claim 2
 An example of timer circuit block diagram is shown in Fig.2. Here, we use two four bit counters to generate 16 intervals per timer. One can use 3 bit or 5 bit counter if the interval needs to be reduced or increased. The upper coarse timer is controlled by a start/stop signal. The counter starts to count only when the BIST sends out START and NOT STOP signals. Each clock period is a single test also issued by the BIST circuit.

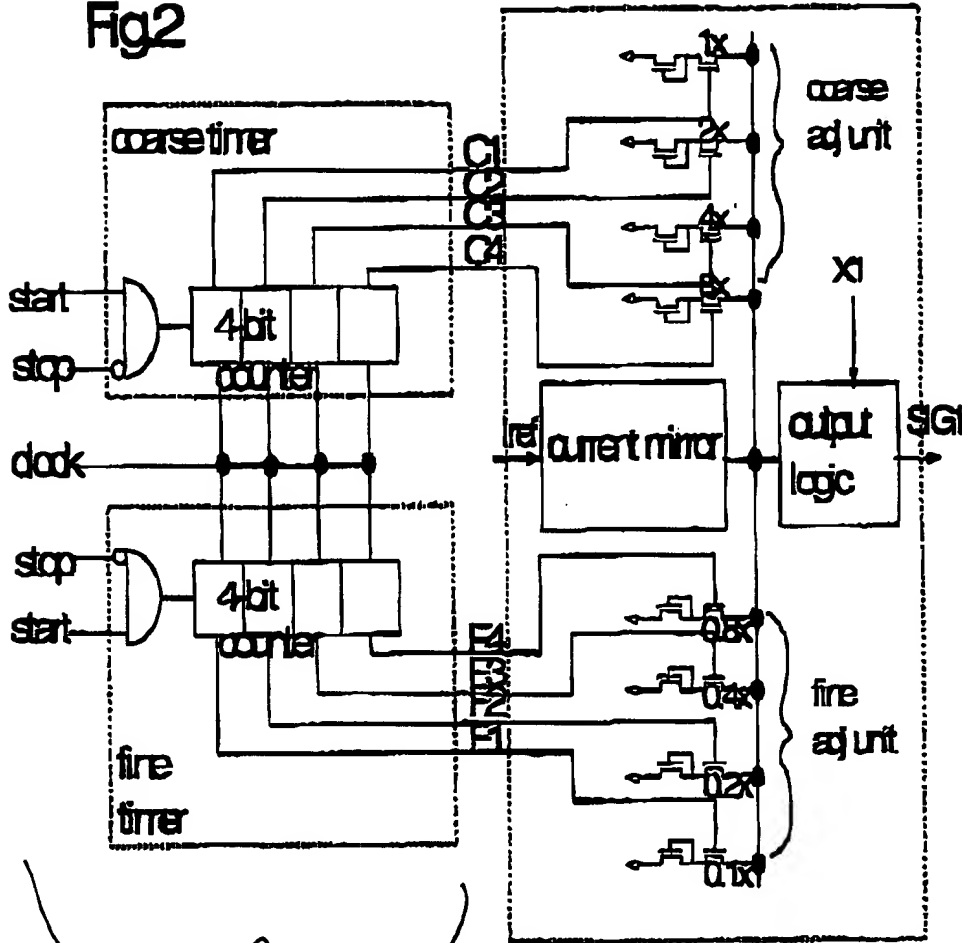


As shown in Fig.3, each 4-bit counter will decrement the timing by n times of the interval. The interval is set by size of the timing adjustment unit. The details of this circuit has been described in another disclosure (eDRAM #5). C1, C2, C3, C4 are output digits from the coarse timer. For example, when C1=1, C2=1, C3=0 and C4=0, then a timing of 3X of the unit delay time is produced at output "SIG1". The unit delay time of the coarse timer is in the range of 5ns, therefore a fine timer is needed for increased resolution. According to the flowchart shown in Fig1, when the coarse timer is stopped (latched), the fine timer is activated, and counting is triggered by the clock. For each test, if the result is negative, the clock will trigger the fine timer to decrease the fine time by an interval. The interval of the fine timer is in the range of 0.5ns. The fine time adjustment unit is built similar to that of the coarse time adjustment unit, except the device sizes are smaller. Using current loading to adjust the time delay is a summation operation. The final timing adjustment is the sum of coarse adjustment plus fine adjustment. First pass on the fine time testing will stop the testing. If an another even finer timer is included, and same operation will continue to get more accurate access time reading.

Such test methodology can apply to almost any kind of circuit timing analysis. For example, to estimate a clock frequency of a micro-process chip, memory array access timing, cycle time, etc.

Claims
3, 4, 5
Control unit

Fig2



4-bit
counters
claim 7

Fig.3

Coarse					Fine				
1X	2X	4X	8X		.1X	.2X	.4X	.8X	
0	0	0	0	0x	0	0	0	0	0x
1	0	0	0	1x	1	0	0	0	.1x
0	1	0	0	2x	0	1	0	0	.2x
1	1	0	0	3x	1	1	0	0	.3x
0	0	1	0	4x	0	0	1	0	.4x
1	0	1	0	5x	1	0	1	0	.5x
0	1	1	0	6x	0	1	1	0	.6x
1	1	1	0	7x	1	1	1	0	.7x
0	0	0	1	8x	0	0	0	1	.8x
1	0	0	1	9x	1	0	0	1	.9x
0	1	0	1	10x	0	1	0	1	.10x
1	1	0	1	11x	1	1	0	1	.11x
0	0	1	1	12x	0	0	1	1	.12x
1	0	1	1	13x	1	0	1	1	.13x
0	1	1	1	14x	0	1	1	1	.14x
1	1	1	1	15x	1	1	1	1	.15x

1x= 5ns

0.1x= 0.5ns

Possible Claims:

1. Chip automatic testing methodology comprising at least two level of timing analysis, the first level analysis is a coarse timing measurement, while the second level analysis is a fine timing measurement.

2. Chip automatic testing apparatus comprising at least two level of timing analysis circuits, the first level analysis circuits performs a coarse timing measurement, while the second level analysis circuit performs a fine timing measurement.

3. Chip automatic testing algorithm comprising at least two level of timing analysis, the tester starts at a predetermined starting timing unit via first level coarse timing analysis. The coarse timer is

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incremented (or decremented) if the chip fails (or passes) during the first test. The test continues until the chip changes state from fail (or pass) to pass (or fail). Then, the tester starts at the current timing index via second level fine timing analysis. The fine timer is incremented (or decremented) if the chip fails (or passes) during the first test. The test continues until the chip changes state from fail (or pass) to pass (or fail). Both coarse and fine timing index are recorded by the tester and read out when the testing is finished.

4. The testing apparatus further comprising at one n-bit counter and at least one timing adjustment circuits, wherein said n-bit counter increments or decrements the testing step of said timing adjustment circuits.

5. N-bit counter referring in claim 4 wherein N is in the range from 2 to 5 depending on the desirable number of timing intervals per test.

6. Timing analysis algorithm referring to claim 3 is included in an on-chip built-in self-test circuit (or BIST). It controls the start and stop operation of each timing analyzer.